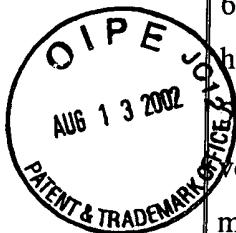


**REMARKS**

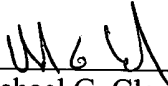
Claim 78 being added by this Amendment is a copy of claim 5 of U.S. Patent No. 6,275,436 of Tobita et al., granted issued August 14, 2002, a copy of which is being filed herewith. Claim 79 being added by this Amendment is modelled on and corresponds to claim of U.S. Patent No. 6,275,436 of Tobita et al. These claims are directed to the use of a non-volatile storage device having both a cache memory and flash memory, where the flash memory serves as the principle memory of the storage device. A prompt examination and allowance is earnestly solicited.



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Respectfully submitted,

  
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8/13/2002  
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## Appendix

### Pending Claims

(Claims 1-62 have been cancelled.)

63. For an electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential, electrons being capable of being injected into the floating gate from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the multi-level memory cells of the second group being substantially flowing in a same direction, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:

settling a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell,

verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter, and of repeating the operation for settling the parameter and the operation for verifying until it is verified by the operation for verifying that the parameter of the one non-volatile multi-level memory cell has being settled to the one state.

reading status of the one non-volatile multi-level memory cell by comparing the parameter with a plurality of reading reference parameters including at least a first reading

reference parameter, a second reading reference parameter and a third reading reference parameter,

wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the second state, the third state and the fourth state,

wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state,

wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,

wherein the normal read operation is carried out by parallel-comparing the parameter with the plurality of reading reference parameters by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter, and

wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.

64. The method of operating the electrically alterable non-volatile multi-level memory according to claim 63, wherein the operation for settling the parameter includes a program operation in which electrons are injected into a floating gate of the one non-volatile multi-level memory cell.

65. For an electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential, electrons being capable of being injected into the floating gate from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the multi-level memory cells of the second group being substantially flowing in a same direction, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:

controlling an electrical value of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell,

verifying whether the electrical value of the one non-volatile multi-level memory cell has being controlled to the one state selected from the plurality of states by comparing the electrical value of the one non-volatile multi-level memory cell with a plurality of verifying reference electrical values including at least a first verifying reference electrical value, a second verifying reference electrical value, a third verifying reference electrical value and a fourth verifying reference electrical value, and of repeating the operation for controlling the electrical value and the operation for verifying until it is verified by the operation for verifying that the electrical value of the one non-volatile multi-level memory cell has being controlled to the one state,

reading status of the one non-volatile multi-level memory cell by comparing the electrical value with a plurality of reading reference electrical values including at least a first reading reference electrical value, a second reading reference electrical value and a third reading reference electrical value,

wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the second state, the third state and the fourth state,

wherein the first reading reference electrical value is allocated between the first state and the second state, the second reading reference electrical value is allocated between the second state and the third state, and the third reading reference electrical value is allocated between the third state and the fourth state,

wherein the first reading reference electrical value, the second reading reference electrical value and the third reading reference electrical value are electrical values for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,

wherein the normal read operation is carried out by parallel-comparing the electrical value with the plurality of reading reference electrical values by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the electrical value from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference electrical value, a second input terminal of the second sense circuit is supplied with the second reading reference electrical value and a second input terminal of the third sense circuit is supplied with the third reading reference electrical value, and

wherein the first verifying reference electrical value is allocated below the first reading reference electrical value, the second verifying reference electrical value is allocated between the first reading reference electrical value and the second reading reference electrical value, the third verifying reference electrical value is allocated between the second reading reference electrical value and the third reading reference electrical value and the fourth verifying reference electrical value is allocated above the third reading reference electrical value.

66. The method of operating the electrically alterable non-volatile multi-level memory according to claim 65, wherein the operation for controlling the electrical value includes a program operation in which electrons are injected into a floating gate of the one non-volatile multi-level memory cell.

67. An electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold

value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential, electrons being capable of being injected into the floating gate from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the multi-level memory cells of the second group being substantially flowing in a same direction:

wherein an operation for settling a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state is carried out in response to information to be stored in the one non-volatile multi-level memory cell,

wherein an operation of verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states is carried out by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter is carried out, and repeating the operation for settling the parameter and the operation for verifying are carried out until it is verified by the operation for verifying that the parameter of the one non-volatile multi-level memory cell has being settled to the one state,

wherein an operation of reading status of the one non-volatile multi-level memory cell is carried out by comparing the parameter with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter,

wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the second state, the third state and the fourth state,

wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state

and the third state, and the third reading reference parameter is allocated between the third state and the fourth state,

wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,

wherein the normal read operation is carried out by parallel-comparing the parameter with the plurality of reading reference parameters by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter, and

wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.

68. The electrically alterable non-volatile multi-level memory according to claim 67, wherein the operation for settling the parameter includes a program operation in which electrons are injected into a floating gate of the one non-volatile multi-level memory cell.

69. The electrically alterable non-volatile multi-level memory according to claim 68, further comprising, a plurality of bit lines, including said first and said second bit line, each of which transfers information indicating data stored in a memory cell, wherein drain regions of said multi-level memory cells of said first group in said matrix are coupled to said first bit line of said plurality of bit lines, drain regions of said multi-level memory cells of said second group adjoining to said first group in said matrix are coupled to said second bit line adjoining to said first bit line in said plurality of bit lines and drain regions of multi-level memory cells

of a third group adjoining to said second column in said matrix are coupled to a third bit line adjoining to said second bit line in said plurality of bit lines

70. An electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential, electrons being capable of being injected into the floating gate from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the multi-level memory cells of the second group being substantially flowing in a same direction:

wherein an operation for controlling an electrical value of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state is carried out in response to information to be stored in the one non-volatile multi-level memory cell,

wherein an operation for verifying whether the electrical value of the one non-volatile multi-level memory cell has being controlled to the one state selected from the plurality of states is carried out by comparing the electrical value of the one non-volatile multi-level memory cell with a plurality of verifying reference electrical values including at least a first verifying reference electrical value, a second verifying reference electrical value is carried out, a third verifying reference electrical value and a fourth verifying reference electrical value, and repeating the operation for controlling the electrical value and the operation for verifying are carried out until it is verified by the operation for verifying that the electrical value of the one non-volatile multi-level memory cell has being controlled to the one state,

wherein an operation for reading status of the one non-volatile multi-level memory cell is carried out by comparing the electrical value with a plurality of reading reference



electrical values including at least a first reading reference electrical value, a second reading reference electrical value and a third reading reference electrical value,

wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the second state, the third state and the fourth state,

wherein the first reading reference electrical value is allocated between the first state and the second state, the second reading reference electrical value is allocated between the second state and the third state, and the third reading reference electrical value is allocated between the third state and the fourth state,

wherein the first reading reference electrical value, the second reading reference electrical value and the third reading reference electrical value are electrical values for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,

wherein the normal read operation is carried out by parallel-comparing the electrical value with the plurality of reading reference electrical values by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the electrical value from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference electrical value, a second input terminal of the second sense circuit is supplied with the second reading reference electrical value and a second input terminal of the third sense circuit is supplied with the third reading reference electrical value, and

wherein the first verifying reference electrical value is allocated below the first reading reference electrical value, the second verifying reference electrical value is allocated between the first reading reference electrical value and the second reading reference electrical value, the third verifying reference electrical value is allocated between the second reading reference electrical value and the third reading reference electrical value and the fourth verifying reference electrical value is allocated above the third reading reference electrical value.

71. The electrically alterable non-volatile multi-level memory according to claim 70, wherein the operation for controlling the electrical value includes a program operation in which electrons are injected into a floating gate of the one non-volatile multi-level memory cell

72. The electrically alterable non-volatile multi-level memory according to claim 71, further comprising, a plurality of bit lines, including said first and said second bit line, each of which transfers information indicating data stored in a memory cell, wherein drain regions of said multi-level memory cells of said first group in said matrix are coupled to said first bit line of said plurality of bit lines, drain regions of said multi-level memory cells of said second group adjoining to said first group in said matrix are coupled to said second bit line adjoining to said first bit line in said plurality of bit lines and drain regions of multi-level memory cells of a third group adjoining to said second column in said matrix are coupled to a third bit line adjoining to said second bit line in said plurality of bit lines.

73. An electrically non-volatile multi-level memory device comprising:  
a plurality of memory cells disposed in matrix having rows and columns,  
wherein each of said plurality of memory cells has a threshold voltage corresponding to data of two bits,

wherein threshold voltages of said plurality of memory cells are allocated to one of a first, a second, a third and a fourth threshold range,

wherein said first threshold range indicates an erase state, and said second, said third, said fourth threshold range indicate program states different from said erase state,

wherein said second, said third and said fourth threshold range indicate mutually different programming states,

wherein a threshold voltage of a memory cell selected from said plurality of memory cells is allocated in one of said first, said second and said third threshold range, and

wherein control gates of memory cells on the same row in said matrix are coupled to a word line of a plurality of word lines,

a plurality of bit lines each of which transfers information indicating data stored in a memory cell, wherein drain regions of memory cells on a first column in said matrix are coupled to a first bit line of said plurality of bit lines, drain regions of memory cells on a second column adjoining to said first column in said matrix are coupled to a second bit line adjoining to said first bit line in said plurality of bit lines and drain regions of memory cells on a third column adjoining to said second column in said matrix are coupled to a third bit line adjoining to said second bit line in said plurality of bit lines,

a programming circuit programming ones of said plurality of memory cells to said programming states by using verify reference parameters,

a sense circuit which compares information indicating data stored in a memory cell with a first reference parameter, a second reference parameter and a third reference parameter in parallel, in a normal read operation,

wherein said first threshold range is lower than said second threshold range, said second threshold range is lower than said third threshold range, and said third threshold range is lower than said fourth threshold range,

wherein said third reference parameter is higher than said second reference parameter, and said second reference parameter is higher than said first reference parameter,

wherein said verify reference parameters have at least first and second verify reference parameters,

wherein said first verify reference parameter is allocated between said second threshold range and said third threshold range, and said second verify reference parameter is allocated between said first threshold range and said second threshold range, and

wherein said first verify reference parameter is settled between said second reference parameter and said third reference parameter, and said second verify reference parameter is settled between said first reference parameter and said second reference parameter

74. An electrically non-volatile multi-level memory device according to claim 73, wherein each of said plurality of memory cells has a floating gate, and a threshold voltage of a selected memory cell is allocated to one of said first, said second and said third threshold range from said fourth threshold range by being injected with hot electron to a floating gate of said selected memory cell

75. An electrically non-volatile multi-level memory device according to claim 74, further comprising,

a column select circuit which receives column addresses, and which couples selected bit lines to said sense circuits

76. An electrically non-volatile multi-level memory device according to claim 75, wherein each of said sense circuits has a first comparator which receives said information and said first reference parameter, a second comparator which receives said information and said

second reference parameter and a third comparator which receives said information and said third reference parameter



77. An electrically non-volatile multi-level memory device according to claim 75, wherein each of said plurality of memory cells has a source region to which is supplied with a reference potential in said read operation.

78.(New) A storage device used for an information processing device comprising:  
a cache memory operably connected to a CPU of said information processing device;  
and

a flash memory operably connected to said cache memory and used as a main memory for said storage device.

79.(New) A storage device used for an information processing device comprising:  
a cache memory operably connected to a microprocessor of said information processing device; and

a flash memory operably connected to said cache memory and used as a primary memory for said storage device.

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